Remarks

Reconsideration of the above-captioned application is respectfully requested. Claims 1-3, 5-14, and 17-25 have been rejected under 35 U.S.C. §103 as being unpatentable over Ishtiaq et al. in view of Zhao et al., Claims 4, 15, and 16 have been rejected under 35 U.S.C. §103 as being unpatentable over Ishtiaq et al. in view of Zhao et al. and further in view of Talluri et al., and Claim 16 has been objected to, which objection is corrected herein.

The enclosed Rule 131 declaration swears behind Ishtiaq et al., removing the rejections.

Further, Applicant does not agree that the references suggest the present claims. As but one example, Ishtiaq et al. does not appear to teach or suggest the iterative smoothing routine set forth in Claim 1 using previous macroblocks to the macroblock at which an error occurred. Instead, Ishtiaq et al., paragraphs [0031] and [0040] appears to conceal errors only in macroblocks subsequent to the macroblock in which the error occurred in a non-iterative fashion.

Additionally, Applicant does not acquiesce that the references alone or in combination teach or suggest the dependent claims. Moreover, Applicant asserts that no prior art reason to combine the references as proposed exists. Ishtiaq et al., for instance, is not directed to the field of Zhao et al., namely, allocating bit rates, but rather to error concealment. There is no suggestion in Ishtiaq et al. that principles in the bit allocation field may be resorted to, nor is there any suggestion in Zhao et al. that its principles may be applied to macroblock error concealment techniques. Indeed, Zhao et al. mentions conventional error concealment in macroblocks but fails to suggest that its bit rate allocation techniques somehow be implemented in them.
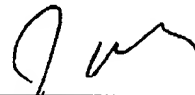
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The Examiner is cordially invited to telephone the undersigned at (619) 338-8075 for any reason

which would advance the instant application to allowance.

Respectfully submitted,

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